# Application of a Three-level NPC Inverter as a Three-Phase Four-Wire Power Quality Compensator by Generalized 3DSVM

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***Abstract*—A two-level four-leg inverter has been developed for the three-phase four-wire power quality compensators. When it is applied to medium and large capacity compensators, the voltage stress across each switch is so high that the corresponding $dv/dt$ causes large electromagnetic interference. The multilevel voltage source inverter topologies are good substitutes, since they can reduce voltage stress and improves output harmonic contents. The existing three-level neutral point clamped (NPC) inverter in three-phase three-wire systems can be used in three-phase four-wire systems also, because the split dc capacitors provide a neutral connection. This paper presents a comparison study between the three-level four-leg NPC inverter and the three-level NPC inverter. A fast and generalized applicable three-dimensional space vector modulation (3DSVM) is proposed for controlling a three-level NPC inverter in a three-phase four-wire system. The zero-sequence component of each vector is considered in order to implement the neutral current compensation. Both simulation and experimental results are given to show the effectiveness of the proposed 3DSVM control strategy. Comparisons between the 3DSVM and the 3-D hysteresis control strategy are also achieved.**

***Index Terms*—Power quality, three-dimensional space vector modulation (3DSVM), three-level neutral point clamped (NPC) inverter, three-phase four-wire system.**

## I. Introduction

DUE to the development of the "custom power" concept, three-phase four-wire systems will play a very important role in the distribution site. Past research shows that there are mainly two ways to provide neutral current compensation by two-level voltage-source inverters (VSIs): 1) using split dc-link capacitors and tying the neutral point to the mid-point of the dc-linked capacitors [1]–[3] and 2) using a four-leg inverter topology and tying the neutral point to the mid-point of the fourth neutral leg [4], [5].

For the medium and large capacity power quality compensators, the multilevel VSI topologies are good alternatives, among which the three-level inverter is the most promising one. The three-level structure not only reduces voltage stress across the switches but also provides more available vectors, which can improve harmonic contents of the VSI by selecting appropriate switching vectors [6], [7]. The decreasing voltage stress leads to corresponding decrease of $dv/dt$, which can reduce the electromagnetic interference (EMI).

The three-level neutral-point-clamped (NPC) inverter, widely used in applications for a three-phase three-wire system, originally has the structure of split dc capacitors. So the existing dc neutral point can be directly utilized as the ground return. Actually, the three-level NPC inverter can be used in applications for a three-phase three-wire system and for a three-phase four-wire system. In this paper, comparisons between the three-level four-leg NPC inverter and the three-level NPC inverter are given in Section II, and the three-level NPC inverter is chosen as a shunt power quality compensator for a three-phase four-wire system.

When the VSI is applied to a shunt power quality compensator, it is the output current of the inverter that needs to be controlled. Various techniques of current control of pulse-width modulation (PWM) inverters have been studied and reported in literature [8], [9]. They can be classified into two large classes: on–off control and predictive control. In on-off control schemes, currents are compared to their reference using hysteresis comparators to determine the switching instants for the inverter power switches. The on–off control is characterized by a fast response but the current ripple is relatively large. In addition, its switching frequency depends on system parameters and operating conditions. On the other hand, in a predictive control scheme the switching instants of power switches are determined through calculating the required voltage to force the output currents to follow the references. This control scheme provides constant switching frequency and lower current ripples. However, injecting circuit parameters and operating conditions have to be known with sufficient accuracy in the predictive control strategy.

Space vector modulation (SVM) techniques have been widely used in predictive control for shunt power quality compensators in a three-phase three-wire system, as this PWM technique can reduce commutation losses and the harmonic contents of output voltage, and can obtain higher amplitude modulation indexes [5], [6]. Usually, SVM can increase 15% of dc voltage utilization compared with sinusoidal PWM. Moreover, space vector modulation techniques can be easily implemented in digital processors.

Corresponding to the adoption of the inverter structure with neutral-wire, three-dimensional (3-D) PWM techniques should be developed for applications in a three-phase four-wire system.

Manuscript received September 27, 2004; revised August 29, 2005. Recommended by Associate Editor P. M. Barbosa.

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Digital Object Identifier 10.1109/TPEL.2005.869755

Two 3-D hysteresis control strategies [10], [11] have been proposed for controlling three-level NPC inverters in shunt power quality compensators. Three-dimensional space vector modulation (3DSVM) for two-level four-leg inverters and three-leg center-split inverters are proposed in 2002 [5] and 2004 [3], respectively. One generalized two-dimensional space vector modulation (2DSVM) has been proposed in [12], which is based on $\alpha$-$\beta$ transformation. However, there is no generalized 3DSVM in $\alpha$-$\beta$-0 coordinates until now.

In Section III a generalized 3DSVM is proposed. The reference voltage vector is decomposed into an offset vector and a two-level vector in the proposed 3DSVM control strategy. The complicated multilevel 3DSVM issue is simplified into a general two-level 3DSVM issue. The control algorithm and computational cost of the proposed 3DSVM control strategy is independent of the levels of the converter. Simulation results are given to show the validity of the proposed control strategy in Section IV, when a three-level NPC inverter is applied as a power quality compensator in a three-phase four-wire system. The comparison with 3-D hysteresis PWM control strategy [10] is also given in Section IV.

In a three-level NPC inverter, the capacitors splitting neutral point voltage has to maintain half bus voltage with respect to either positive or negative bus. However, the variation of neutral point voltage is inevitable especially when the neutral current is compensated. All the space vector neutral point balancing strategies [13] for conventional three-level inverters can be used in this novel 3DSVM, so that the dc voltage variation control is not considered in this paper.

In the last part of the paper, the proposed 3DSVM is applied to a shunt power quality compensator prototype, in which a three-level NPC inverter is used. Experimental results proved that harmonics, reactive current, and neutral current can be compensated simultaneously when the proposed 3DSVM is employed.

## II. Comparison of Three-Level Four-Leg and Three-Leg NPC Inverter

A three-level NPC inverter and a three-level four-leg NPC inverter are shown in Fig. 1(a) and (b), respectively. Both of the two inverters can be used as a shunt power quality compensator for three-phase four-wire systems as shown in Fig. 1. The number of the components in each inverter is listed in Table I. Since a fourth leg is added to provide the neutral connection, the three-level four-leg NPC inverter needs more insulated gate bipolar transistor (IGBT) switches, diodes, snubber circuits, etc., than a conventional three-level inverter needs.

In order to compare the compensation performance of the two three-level NPC inverters, the output space vectors of each inverter should be determined first.

First, the switching function of the three-level inverter is defined as

$$S_j = \begin{cases} 1, & \text{when } T_{1j} \text{ and } T_{2j} \text{ are conducting} \\ 0, & \text{when } T_{2j} \text{ and } T_{3j} \text{ are conducting } j = a, b, c, n \\ -1, & \text{when } T_{3j} \text{ and } T_{4j} \text{ are conducting .} \end{cases} \tag{1}$$

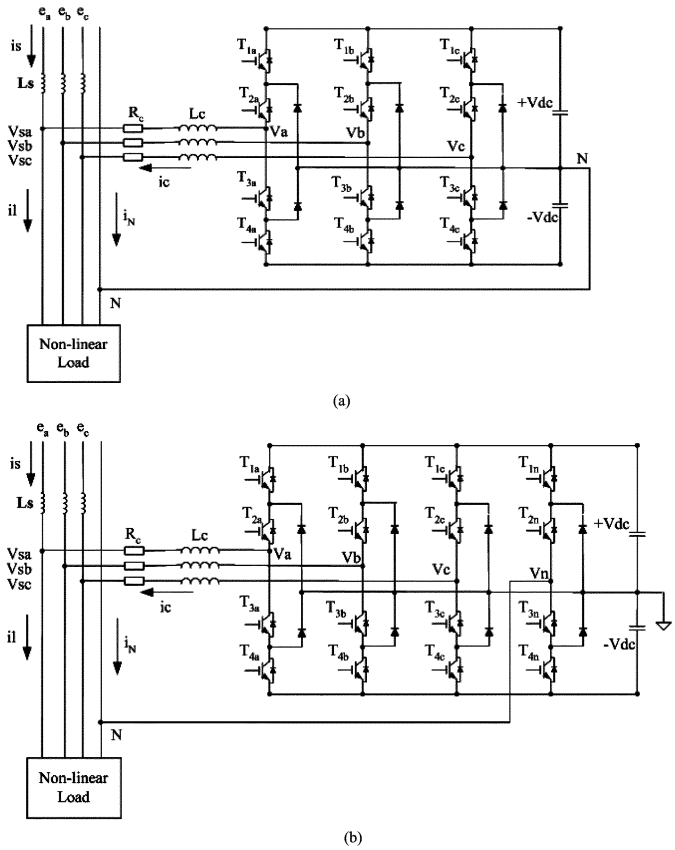


Fig. 1. Three-level NPC inverter for a three-phase four-wire system: (a) three-leg structure and (b) four-leg structure.

TABLE I
Comparison of Numbers of Components

| | IGBT Switches | Clamped diodes | capacitors |
|---|---|---|---|
| Three-level 3-Leg NPC VSI | 12 | 6 | 2 |
| Three-level 4-Leg NPC VSI | 16 | 8 | 2 |

It is assumed that the upper-leg and lower-leg capacitor voltages of both two inverters are $V_{\rm dc}$. Hence, the output voltage of each leg can be expressed as

$$v_j = V_{\rm dc} * S_j \quad j = a, b, c, n. \tag{2}$$

$v_j$ represents the output voltage of each leg. However, it is the phase to neutral voltage, which determines the output of the inverter. The output phase to neutral voltage of the inverter is defined as

$$v_{jn} = v_j - v_n, \quad j = a, b, c. \tag{3}$$

The output voltage vector of the inverter in $a$-$b$-$c$ coordinates is expressed as

$$\vec{v} = \sqrt{\frac{2}{3}} \left( v_{an} + \alpha \cdot v_{bn} + \alpha^2 \cdot v_{cn} \right) \tag{4}$$

where $\alpha = e^{j(2\pi/3)}$, $\alpha^2 = e^{-j(2\pi/3)}$.

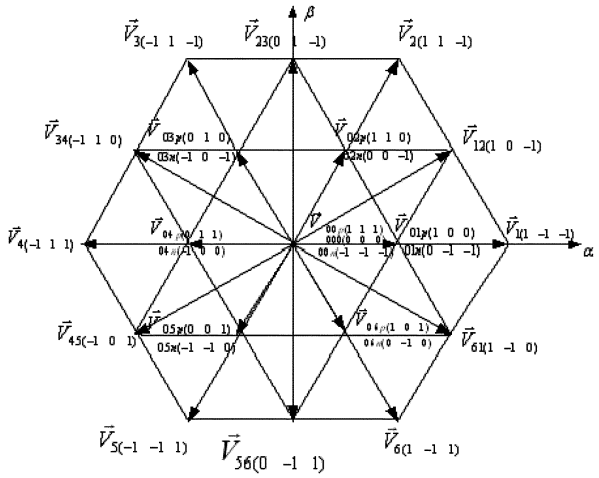

Fig. 2. Space vector allocation on $\alpha$-$\beta$ plane of a three-level NPC inverter.

According to the $\alpha$-$\beta$-0 transformation in (5), the instantaneous voltage vector in the $\alpha$-$\beta$-0 frame is given as

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{5}$$

$$\vec{v} = (v_\alpha \cdot \vec{n}_\alpha + v_\beta \cdot \vec{n}_\beta + v_0 \cdot \vec{n}_0), \text{where} \tag{6}$$

$$\begin{cases} v_\alpha = \sqrt{\frac{2}{3}} \left( v_{an} - \frac{1}{2} v_{bn} - \frac{1}{2} v_{cn} \right) \\ v_\beta = \frac{1}{\sqrt{2}} (v_{bn} - v_{cn}) \\ v_0 = \frac{1}{\sqrt{3}} (v_{an} + v_{bn} + v_{cn}). \end{cases} \tag{7}$$

If (3) is substituted to (7), the following results can be obtained:

$$\begin{cases} v_\alpha = \sqrt{\frac{2}{3}} \left( v_a - \frac{1}{2} v_b - \frac{1}{2} v_c \right) \\ v_\beta = \frac{1}{\sqrt{2}} (v_b - v_c) \\ v_0 = \frac{1}{\sqrt{3}} ((v_a + v_b + v_c) - 3v_n). \end{cases} \tag{8}$$

It can be seen from (8) that the $\alpha$- and $\beta$-axis components of the output voltage vector are only determined by the output voltage of leg A, B, and C, i.e., the switching state of leg A, B, and C. If the switching state of leg A, B, and C of the two inverters are the same, the $\alpha$ and $\beta$ axes output of the four-leg and the three-leg inverter are the same. There are 27 vectors corresponding to the different switching state combinations of leg A, B, and C. The space vector allocations on the $\alpha$-$\beta$ plane for a four-leg and a three-leg inverter are the same, as shown in Fig. 2.

The difference of the output space vector allocation between a four-leg inverter and a three-leg inverter exists in the zero-axis component $v_0$, which is determined by the output voltage of leg A, B, C and the neutral voltage $v_n$ according to (8). There are totally seven different values for $(v_a + v_b + v_c)$: $(-3\ \mathrm{V_{dc}}, -2\ \mathrm{V_{dc}}, -V_{\mathrm{dc}}, 0, V_{\mathrm{dc}}, 2\ \mathrm{V}_{dc}, 3\ \mathrm{V_{dc}})$. The value of $v_n$ is always equal to "0" in a conventional three-level inverter. So, the zero-axis output of a three-leg inverter has seven possible values and the maximum value is $\pm\sqrt{3}V_{\mathrm{dc}}$. However, the value of $v_n$ can be chosen among $V_{\mathrm{dc}}$, 0 and $-V_{\mathrm{dc}}$ according to the switching state of the fourth leg in a three-level four-leg NPC inverter. Originally, there should be 21 possible zero-axis output values for a four-leg inverter. However, many zero-axis outputs are overlapped. So the zero-axis output of a four-leg inverter has thirteen different possible values and the maximum value is $\pm 2\sqrt{3}V_{\mathrm{dc}}$.

Therefore, following results can be obtained based on the previous analyses.

- The four-leg inverter has $3^4 = 81$ different switching states. Although the total number of output voltage vectors increases a lot compared with 27 vectors of a three-leg inverter, the number of different space vectors on $\alpha$-$\beta$ plane doesn't increase. Even in $\alpha$-$\beta$-0 3-D coordinates, some vectors of the three-level four-leg inverter are overlapped although their corresponding switching states are different. The increase of overlapped vectors increases the complexity of PWM control.
- The three-level four-leg NPC inverter and the conventional three-level NPC inverters have the same compensation capability on the $\alpha$-$\beta$ plane. That is to say, when they are used to compensate harmonics in phase currents, their dc voltage utility ratio is the same.
- Compared with the three-leg inverter, the four-leg inverter doubles the maximum output on zero-axis. So, the neutral current compensation capability of a four-leg inverter is higher. In addition, the four-leg inverter has higher flexibility on zero-sequence compensation, as it has more possible zero-axis output values.

However, the initial cost of a four-leg inverter increases a lot because more switching components, pulse triggered terminals, drives and even controllers are needed. For example, if TI TMS320F2407 DSP Controller is chosen to generate the PWM trigger signal, only one DSP chip is enough for controlling a three-level three-leg inverter. However, extra hardware or controllers are needed for controlling a four-leg inverter, which increases the complexity of implementation.

In a word, both a three-level four-leg NPC inverter and a three-level NPC inverter can be used to compensate the neutral current in a three-phase four-wire system. The three-level NPC inverter is cheaper and easier to control. Hence, in this paper the three-level NPC inverter is used in a shunt power quality compensator and a generalized 3DSVM control strategy is proposed for this inverter topology.

## III. Generalized 3DSVM for Three-Level Three-Leg NPC Inverter

In the 3DSVM for a two-level three-leg center-split inverter [3], all the eight vectors contribute to the zero-sequence compensation, which is different from the conventional 2DSVM. In order to compensate the neutral current, the zero-sequence components of each vector of a three-level NPC inverter need to be considered too. Typically, the SVM techniques for a multilevel inverter lead to large tables of vectors and awkward mathematical relationships. In this section, a generalized 3DSVM is proposed, in which the complicated multilevel 3DSVM control is greatly simplified. The reference voltage vector is decomposed to an offset vector and a two-level vector. Important issues for 3DSVM, such as identification of adjacent switching vectors, switching sequences schemes and dwell time calculations are

all settled by a general two-level 3DSVM. The detailed procedure of the generalized 3DSVM is given hereinafter.

### *A. Normalization of Space Vectors*

Each phase output voltage of a three-level three-leg NPC inverter can be expressed as

$$v_j = V_{\rm dc} * S_j \quad j = a, b, c.$$

Since the neutral voltage $v_n$ equals to zero in a three-level NPC inverter, $v_j$ equals to the phase to neutral voltage $v_{jn}$. All the voltage vectors are represented in per unit, i.e., normalized by $V_{\rm dc}$, so that the output voltage of each leg has the same value as the corresponding switching state. The normalization makes it more convenient for determining the neighboring vectors and the final output sequences in the proposed generalized 3DSVM. The output voltage of each phase can be expressed as

$$v_j = S_j \quad j = a, b, c. \tag{9}$$

The reference voltage vector should be normalized by $V_{\rm dc}$ also

$$\vec{v}_{\rm ref} = \frac{\vec{V}_{\rm ref}}{V_{\rm dc}} = \begin{bmatrix} \frac{V_{\rm refa}}{V_{\rm dc}} \\ \frac{V_{\rm refb}}{V_{\rm dc}} \\ \frac{V_{\rm refc}}{V_{\rm dc}} \end{bmatrix}. \tag{10}$$

### *B. Decomposition of Reference Voltage Vectors*

In the proposed 3DSVM, the desired output voltage vector is decomposed into two components as

$$\vec{v}_{\rm ref} = \vec{v}_{\rm offset} + \vec{v}_{twol}. \tag{11}$$

It can also be expressed as (12) in $a$-$b$-$c$ coordinates.

$$\begin{bmatrix} v_{\rm refa} \\ v_{\rm refb} \\ v_{\rm refc} \end{bmatrix} = \begin{bmatrix} v_{\rm offset(a)} \\ v_{\rm offset(b)} \\ v_{\rm offset(c)} \end{bmatrix} + \begin{bmatrix} v_{\rm twol(a)} \\ v_{\rm twol(b)} \\ v_{\rm twol(c)} \end{bmatrix}. \tag{12}$$

The offset component of the reference voltage is defined as

$$\vec{v}_{\rm offset} = \begin{bmatrix} v_{\rm offset(a)} \\ v_{\rm offset(b)} \\ v_{\rm offset(c)} \end{bmatrix} = \begin{bmatrix} Mod(v_{\rm refa}) \\ Mod(v_{\rm refb}) \\ Mod(v_{\rm refc}) \end{bmatrix}, \text{where} \tag{13}$$

$$Mod(v_{\rm refj}) = \begin{cases} Int(v_{\rm refj}) & v_{\rm refj} \geq 0 \\ Int(v_{\rm refj}) - 1 & v_{\rm refj} < 0 \end{cases} \quad j = a, b, c. \tag{14}$$

$Int()$ removes fractional part of the real input data. The two-level component of the reference voltage is defined as

$$\vec{V}_{\rm twol} = \vec{V}_{\rm ref} - \vec{V}_{\rm offset} = \begin{bmatrix} v_{\rm twol(a)} \\ v_{\rm twol(b)} \\ v_{\rm twol(c)} \end{bmatrix}$$
$$\text{where } 0 \leq v_{\rm twol(j)} < 1 \quad (j = a, b, c). \tag{15}$$

If $(v_{\rm offset(a)}, v_{\rm offset(b)}, v_{\rm offset(c)})$ equals to $(S_a, S_b, S_c)$, the reference voltage vector must locate inside a two-level space vector allocation formed by $(S_a, S_b, S_c)$ $(S_a + 1, S_b, S_c)$, $(S_a, S_b + 1, S_c)$, $(S_a, S_b, S_c + 1)$, $(S_a + 1, S_b + 1, S_c)$, $(S_a + 1, S_b, S_c + 1)$, $(S_a, S_b + 1, S_c + 1)$, and $(S_a + 1, S_b + 1, S_c + 1)$. The two-level space vector allocation in $\alpha$-$\beta$-0 coordinates is shown in Fig. 3(a) and its projection on the $\alpha$-$\beta$ plane is shown in Fig. 3(b). It can be seen from Fig. 3(a) that vectors $(S_a + 1, S_b, S_c)$, $(S_a, S_b + 1, S_c)$ and $(S_a, S_b, S_c + 1)$ locate on the same horizontal plane, and vectors $(S_a + 1, S_b + 1, S_c)$, $(S_a + 1, S_b, S_c + 1)$ and $(S_a, S_b + 1, S_c + 1)$ locate on the other horizontal plane. There are four voltage levels or units in the zero-axis in a two-level space vector allocation.

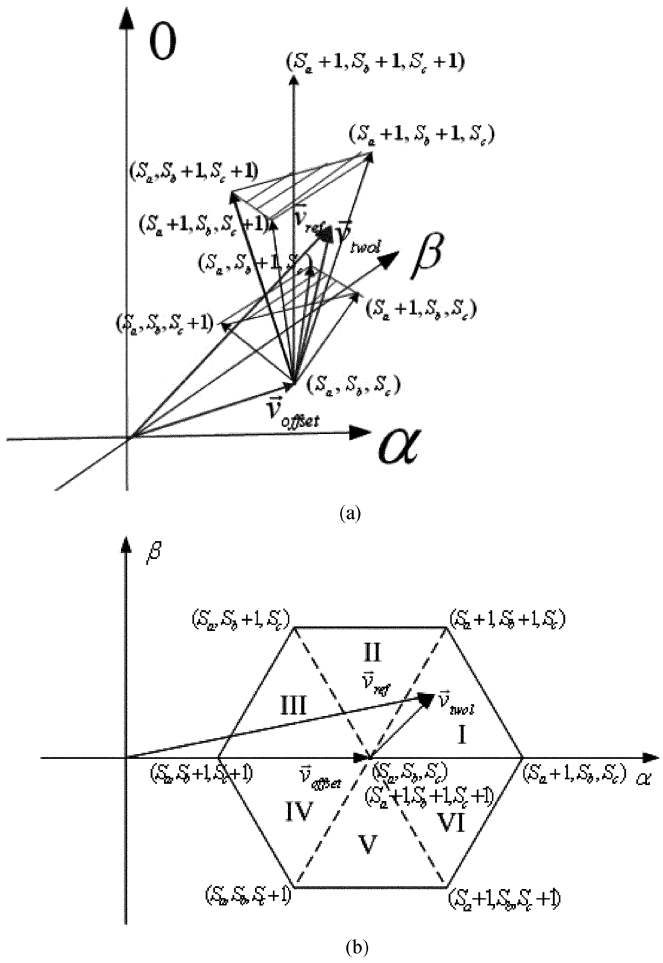


Fig. 3. Space vector allocation of two-level vectors (a) in $\alpha$-$\beta$-0 coordinates and (b) projection on the $\alpha$-$\beta$ plane.

The decomposition of the reference voltage vector is also illustrated in Fig. 3. The 3-D parameters of two-level reference voltage vector can be expressed as (16) according to the $\alpha$-$\beta$-0 transformation in (5)

$$\begin{bmatrix} v_{\rm twol\alpha} \\ v_{\rm twol\beta} \\ v_{\rm twol0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_{\rm twol(a)} \\ v_{\rm twol(b)} \\ v_{\rm twol(c)} \end{bmatrix}. \tag{16}$$

### *C. Determination of Output Switching States*

In the proposed 3DSVM, the reference voltage vector is synthesized by four neighboring vectors

$$\vec{v}_{\rm ref} \cdot T_S = \vec{v}_1 T_1 + \vec{v}_2 T_2 + \vec{v}_3 T_3 + \vec{v}_4 T_4. \tag{17}$$

If the dwell time of each vector is normalized by the sample time $T_s$. The following results can be obtained:

$$\vec{v}_{\rm ref} = \vec{v}_1 t_1 + \vec{v}_2 t_2 + \vec{v}_3 t_3 + \vec{v}_4 t_4 \tag{18}$$
$$\text{and } t_1 + t_2 + t_3 + t_4 = 1. \tag{19}$$

TABLE II
SWITCHING SEQUENCES OF EACH SUB-SECTOR

| Sequence | $\vec{v}_1$ | $\vec{v}_2$ | $\vec{v}_3$ | $\vec{v}_4$ |
|---|---|---|---|---|
| 1 | $(S_a, S_b, S_c)$ | $(S_a{+}1, S_b, S_c)$ | $(S_a{+}1, S_b{+}1, S_c)$ | $(S_a{+}1, S_b{+}1, S_c{+}1)$ |
| 2 | $(S_a, S_b, S_c)$ | $(S_a, S_b{+}1, S_c)$ | $(S_a{+}1, S_b{+}1, S_c)$ | $(S_a{+}1, S_b{+}1, S_c{+}1)$ |
| 3 | $(S_a, S_b, S_c)$ | $(S_a, S_b{+}1, S_c)$ | $(S_a, S_b{+}1, S_c{+}1)$ | $(S_a{+}1, S_b{+}1, S_c{+}1)$ |
| 4 | $(S_a, S_b, S_c)$ | $(S_a, S_b, S_c{+}1)$ | $(S_a, S_b{+}1, S_c{+}1)$ | $(S_a{+}1, S_b{+}1, S_c{+}1)$ |
| 5 | $(S_a, S_b, S_c)$ | $(S_a, S_b, S_c{+}1)$ | $(S_a{+}1, S_b, S_c{+}1)$ | $(S_a{+}1, S_b{+}1, S_c{+}1)$ |
| 6 | $(S_a, S_b, S_c)$ | $(S_a{+}1, S_b, S_c)$ | $(S_a{+}1, S_b, S_c{+}1)$ | $(S_a{+}1, S_b{+}1, S_c{+}1)$ |

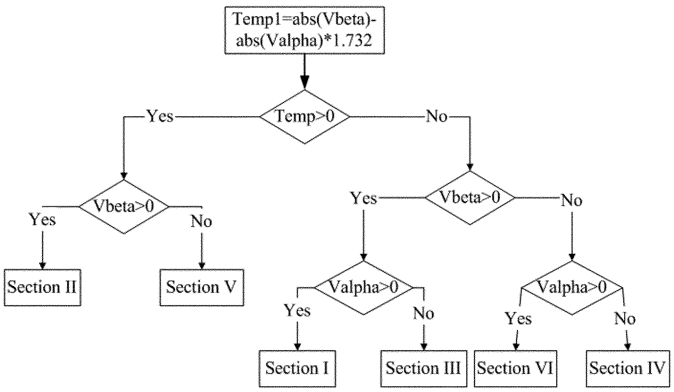


Fig. 4. Choosing the section area.

The vector $\vec{v}_1$ is the offset voltage vector determined by (13), which locates at the center point of the eight vectors on $\alpha$-$\beta$ plane. $\vec{v}_2$ and $\vec{v}_3$ are chosen as the neighboring vectors of the reference voltage vector on the $\alpha$-$\beta$ plane. It can be seen from Fig. 3(b) that the vectors $(S_a, S_b, S_c)$ and $(S_a{+}1, S_b{+}1, S_c{+}1)$ overlap on the $\alpha$-$\beta$ plane. Modifying the dwell times between these two vectors only affect the zero-sequence output. Hence, the zero-sequence compensation is implemented by introducing the fourth vector in reference voltage vector approximation, and $\vec{v}_4$ is always chosen as $(S_a+1, S_b+1, S_c+1)$. This is different from the generalized 2DSVM [12] in which only three neighboring vectors are employed.

Each sector on the $\alpha$-$\beta$ plane, as shown in Fig. 3(b), corresponds to one output switching sequences as the neighboring vectors of reference voltage vector are different. The switching sequences for each sector are listed in Table II.

The angle of the two-level reference voltage vector can be used to detect which sector the reference voltage vector locates in. However, it is not convenient to calculate the angle when the 3DSVM is implemented in a digital controller. Hence, a sector detection algorithm is designed in this paper. A temporary parameter $|v_{twol\beta}| - |v_{twol\alpha}| * \sqrt{3}$ is introduced to determine the section together with the sign of $\alpha$-, $\beta$-axis components. The flow chart of determination of the sector is illustrated in Fig. 4, which can simplify the calculation and reduce the executing time of the program.

TABLE III
TWO-LEVEL 3DPWM VOLTAGE VECTOR'S PARAMETERS

| | $S_a$ | $S_b$ | $S_c$ | $S_\alpha$ | $S_\beta$ | $S_0$ | $v_\alpha$ | $v_\beta$ | $v_0$ |
|---|---|---|---|---|---|---|---|---|---|
| $\vec{V}_t$ | 1 | 0 | 0 | 1 | 0 | 1 | $\sqrt{\frac{2}{3}}$ | 0 | $\frac{1}{\sqrt{3}}$ |
| $\vec{V}_2$ | 1 | 1 | 0 | 0.5 | 1 | 2 | $\sqrt{\frac{1}{6}}$ | $\frac{1}{\sqrt{2}}$ | $\frac{2}{\sqrt{3}}$ |
| $\vec{V}_3$ | 0 | 1 | 0 | -0.5 | 1 | 1 | $-\sqrt{\frac{1}{6}}$ | $\frac{1}{\sqrt{2}}$ | $\frac{1}{\sqrt{3}}$ |
| $\vec{V}_4$ | 0 | 1 | 1 | -1 | 0 | 2 | $-\sqrt{\frac{2}{3}}$ | 0 | $\frac{2}{\sqrt{3}}$ |
| $\vec{V}_5$ | 0 | 0 | 1 | -0.5 | -1 | 1 | $-\sqrt{\frac{1}{6}}$ | $\frac{-1}{\sqrt{2}}$ | $\frac{1}{\sqrt{3}}$ |
| $\vec{V}_6$ | 1 | 0 | 1 | 0.5 | -1 | 2 | $\sqrt{\frac{1}{6}}$ | $\frac{-1}{\sqrt{2}}$ | $\frac{2}{\sqrt{3}}$ |
| $\vec{V}_{00p}$ | 1 | 1 | 1 | 0 | 0 | 3 | 0 | 0 | $\sqrt{3}$ |
| $\vec{V}_{00n}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### *D. Calculation of Dwell Time and Determination of Switching Sequences*

If the offset voltage vector $\vec{v}_{\text{offset}}$ is subtracted from both sides of (18), (20) can be obtained

$$\vec{v}_{twol} = \vec{v}_{1t}t_1 + \vec{v}_{2t}t_2 + \vec{v}_{3t}t_3 + \vec{v}_{4t}t_4. \tag{20}$$

The subscript "$t$" in (20) denotes that the vector is one of the two-level space vectors. The parameters of two-level 3-D space vectors are listed in Table III.

Since both $\vec{v}_{1t}$ (0,0,0) and $\vec{v}_{4t}$ (0,0,3) don't affect the $\alpha$, $\beta$ axis output, $t_2$ and $t_3$ can be calculated by using (21), which is also widely used in 2DSVM [12]

$$\begin{bmatrix} v_{\text{twol}\alpha} \\ v_{\text{twol}\beta} \end{bmatrix} = \begin{bmatrix} v_{2\alpha} & v_{3\alpha} \\ v_{2\beta} & v_{3\beta} \end{bmatrix} \begin{bmatrix} t_2 \\ t_3 \end{bmatrix}. \tag{21}$$

However, it is inconvenient to solve the equation in matrix form in programming. Therefore, the six equations corresponding to six different section areas are solved in advance, and the results can be expressed as following:

$$\text{Section I}: \begin{cases} t_2 = \left(\sqrt{\frac{3}{2}}\right) v_{twol\alpha} - 0.5 \cdot t_3 \\ t_3 = \sqrt{2} v_{\text{twol}\beta} \end{cases}$$

$$\text{Section II}: \begin{cases} t_2 = t_3 - \sqrt{6} v_{\text{twol}\alpha} \\ t_3 = \left(\sqrt{\frac{3}{2}}\right) v_{\text{twol}\alpha} + \left(\frac{\sqrt{2}}{2}\right) v_{\text{twol}\beta} \end{cases}$$

$$\text{Section III}: \begin{cases} t_2 = \sqrt{2} v_{\text{twol}\beta} \\ t_3 = \left(-\sqrt{\frac{3}{2}}\right) v_{\text{twol}\alpha} - 0.5 \cdot t_2 \end{cases}$$

$$\text{Section IV}: \begin{cases} t_2 = -\sqrt{2} v_{\text{twol}\beta} \\ t_3 = \left(-\sqrt{\frac{3}{2}}\right) v_{\text{twol}\alpha} - 0.5 \cdot t_2 \end{cases}$$

$$\text{Section V}: \begin{cases} t_2 = t_3 - \sqrt{6} v_{\text{twol}\alpha} \\ t_3 = \left(\sqrt{\frac{3}{2}}\right) v_{\text{twol}\alpha} - \left(\frac{\sqrt{2}}{2}\right) v_{\text{twol}\beta} \end{cases}$$

$$\text{Section VI}: \begin{cases} t_2 = \left(\sqrt{\frac{3}{2}}\right) v_{\text{twol}\alpha} - 0.5 \cdot t_3 \\ t_3 = -\sqrt{2} v_{\text{twol}\beta} \end{cases}$$

$t_4$ can be calculated according to the zero-sequence component of the two-level vector and the zero-axis output of $\vec{v}_2$ and $\vec{v}_3$ as

$$t_4 = \frac{1}{\sqrt{3}} v_{\text{twol0}} - \frac{1}{3} t_2 - \frac{2}{3} t_3 \tag{22}$$

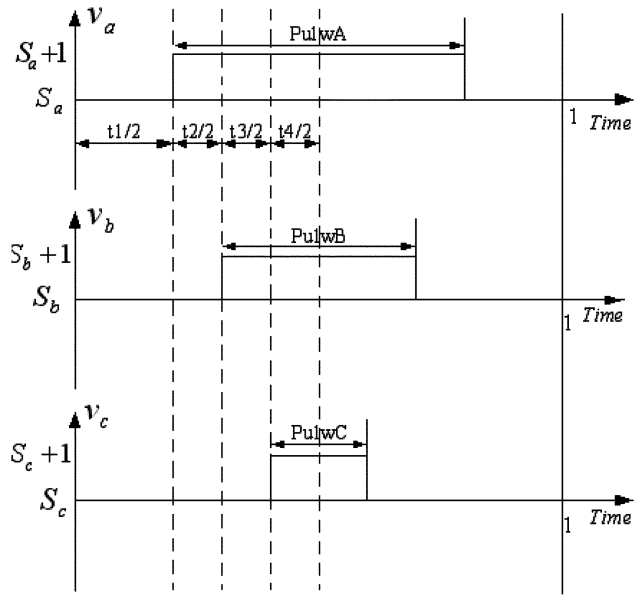


Fig. 5. PWM output for one sampling period.

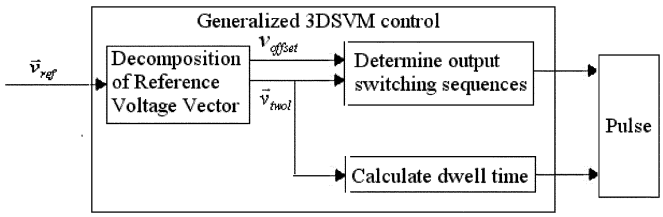


Fig. 6. Control algorithm of generalized 3DSVM control.

$$\text{and } t_1 = 1 - t_2 - t_3 - t_4. \tag{23}$$

Hence, only additions and multiplications are needed in the programming, which also reduces the executing time in digital signal processors.

After the dwell time of each vector is calculated, the final output of the inverter can be determined. The sequencing of switching vectors can be optimized and comparisons among different sequencing schemes are given in [5]. The symmetrically aligned scheme is indicated to give the lowest output voltage distortion and current ripple. So it is chosen in this paper. The switching sequence of the generalized 3DSVM is $\bar{v}_1 \rightarrow \bar{v}_2 \rightarrow \bar{v}_3 \rightarrow \bar{v}_4$ in the first half period and in reverse turn $\bar{v}_4 \rightarrow \bar{v}_3 \rightarrow \bar{v}_2 \rightarrow \bar{v}_1$ for the next half period. Fig. 5 illustrates the output waveform, in which sequence 1 in Table II is used as an example.

### *E. Generalized Control Algorithm*

The control algorithm of the generalized 3DSVM method is shown in Fig. 6. If the 3DSVM is applied to a higher-level system, the algorithm is always the same and the computational cost is independent of the levels of the converter. Therefore, the proposed 3DSVM in this paper can be named a generalized 3DSVM for multilevel systems.

## IV. Simulation Results

The simulation is performed by MATLAB/Simulink. The compensation system configuration is shown in Fig. 1(a), in which a three-level NPC inverter is used as a shunt power quality compensator for a three-phase four-wire system. The peak value of the source voltage is 100 V and $Rc = 2\Omega$, $Lc =$ 12 mH, $V_{\rm dc} = 160$ V. The instantaneous reference current for compensation is determined by the Generalized Instantaneous Reactive Power Theory [14]. The reference voltage vector at time $KT$ is calculated by (24) [11], where $T$ is the fixed sampling period

$$\vec{v}[KT] = \vec{v}_S[KT] - \frac{R_c}{\Delta X}\left\{\vec{i}_c^{\,*}[KT] - (1-\Delta X)\,\vec{i}_c[KT]\right\} \tag{24}$$

where $\Delta X = (R_c/L_c) \cdot e^{-(R_c/L_c)T} \cdot T$.

The three-phase unbalanced nonlinear load, which is used to test the performance of the compensator, is shown in Fig. 7. The parallel power quality compensator begins to operate at 0.02 s. The switches in phase A is turned on at first, and it will be turned off at 0.05 s. The currents passing through the nonlinear loads are shown in Fig. 8.

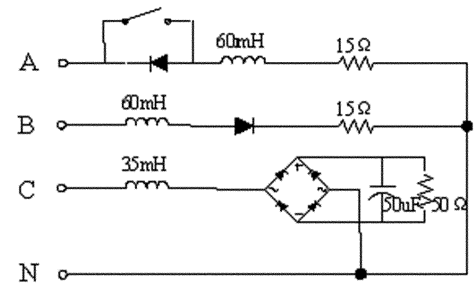


Fig. 7. Three-phase unbalanced nonlinear loads.

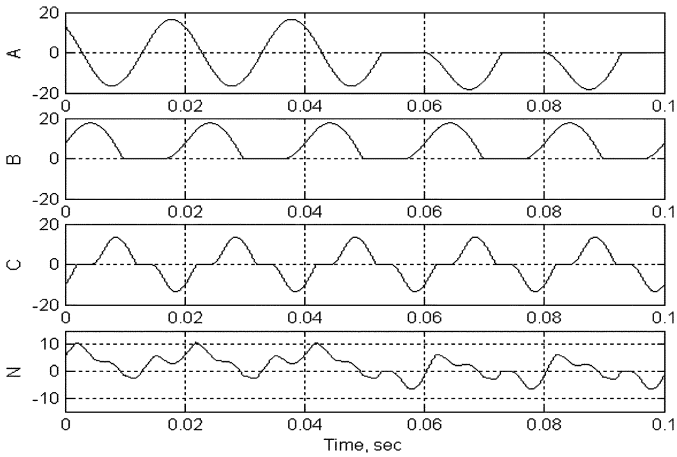


Fig. 8. Load current.

### *A. Simulation Results of 3DSCH Control*

The 3-D sign cubic hysteresis (3DSCH) [10] is implemented to control the shunt power quality compensator. The sampling frequency is 20 kHz. The current after compensation by 3DSCH is shown in Fig. 9. Because the hysteresis PWM is a frequency varying modulation scheme, only an estimated average switching frequency can be detected in simulation, which is about 5.6 kHz.

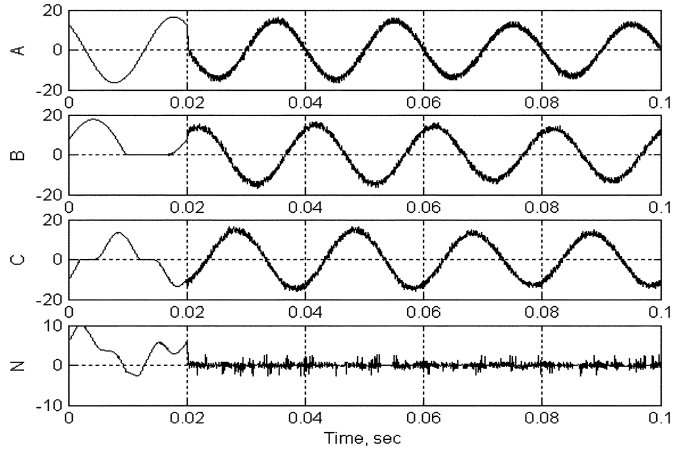


Fig. 9. Some current after compensation by 3DSCH.

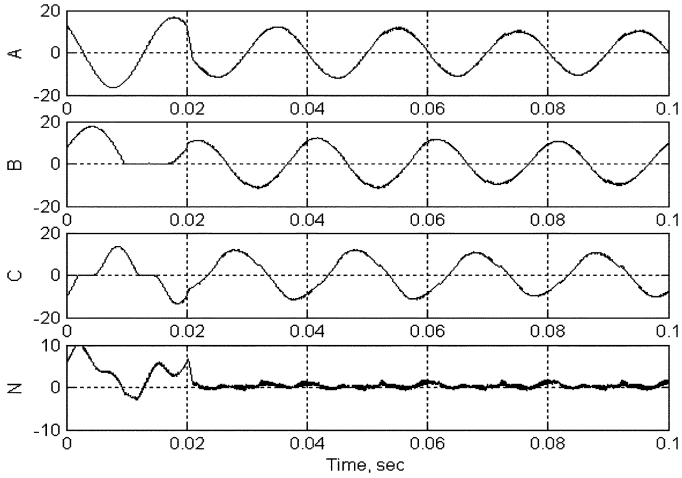


Fig. 10. Source current after compensation by 3DSVM.

### B. Simulation Results of the Proposed Generalized 3DSVM

The proposed 3DSVM is applied to control the three-level NPC inverter and the sampling frequency is 5 KHz. Fig. 10 shows the source current after compensation. It can be seen from Fig. 10 that the neutral current is compensated with three-phase current harmonics, and current unbalances dynamically.

According to Fig. 5, the switching state of each leg of the three-level inverter only changes one level. So, only two of the total four switches of one leg need to operate in one sampling period. For example, if the output switching state changes from "0" to "1," the switches T1j and T3j need to operate and the other two switches T2j and T4j remains the previous state, as indicated in (1). Hence, the switching frequency of each switch is around 2.5 kHz, which is half of the sampling frequency.

### C. Comparisons Between the Two 3DPWM Control Strategies

The total harmonic distortion (THD) values of three phase currents before and after compensation are listed in Table IV. The performance indices are defined as (25)–(28) [11]. The indices $J_\alpha$, $J_\beta$ and $J_0$ are the average absolute errors in the $\alpha$, $\beta$ and 0 axes of one period. The index $J_{\alpha\beta 0}$ is the sum of all absolute mean errors. The objective of compensation is to make all the proposed indices as small as possible. The corresponding compensation indexes are listed in Table IV. The switching frequency detected in the simulation is also listed in Table IV together with the sampling frequency of the control loop

TABLE IV
COMPENSATION PARAMETERS

| Comparison of 3D PWM Techniques | Without Compensation | 3DSCH Control Strategy | 3DSVM Control Strategy |
|---|---|---|---|
| THD of Phase A Current | 28.5% | 8.06% | 5.56% |
| THD of Phase B Current | 28.5% | 7.79% | 5.65% |
| THD of Phase C Current | 35.68% | 7.77% | 8.17% |
| $J\alpha$ | 6.71 | 0.5822 | 0.3372 |
| $J_\beta$ | 4.886 | 0.6636 | 0.2986 |
| $J_0$ | 2.848 | 0.4189 | 0.5000 |
| $J_{\alpha\beta 0}$ | 14.24 | 1.665 | 1.136 |
| Sampling frequency | | 20kHz | 5kHz |
| Averaged switching frequency | | 5.6kHz | 2.5kHz |

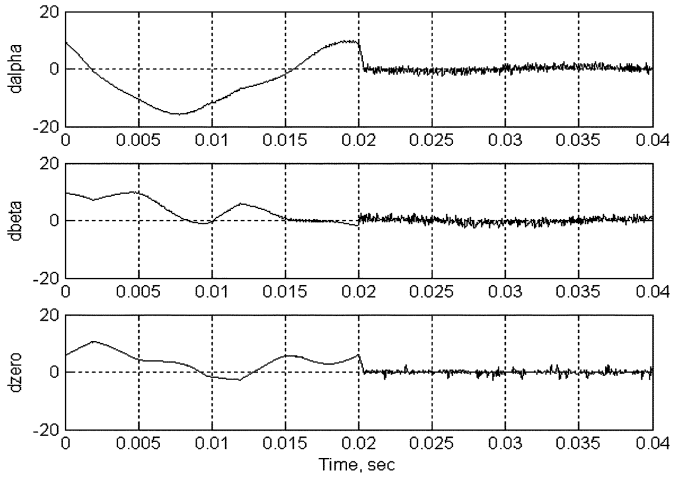


Fig. 11. Compensation error by using 3DSCH.

$$J_\alpha = \frac{1}{T}\int_0^T |\Delta i_\alpha| dt \tag{25}$$

$$J_\beta = \frac{1}{T}\int_0^T |\Delta i_\beta| dt \tag{26}$$

$$J_0 = \frac{1}{T}\int_0^T |\Delta i_0| dt \tag{27}$$

$$J_{\alpha\beta 0} = \frac{1}{T}\int_0^T (|\Delta i_\alpha| + |\Delta i_\beta| + |\Delta i_0|) dt. \tag{28}$$

It can be seen from Table IV that the proposed 3DSVM has better performance on reducing compensation errors on $\alpha$ and $\beta$ axes. The variations of $\Delta i_\alpha$, $\Delta i_\beta$ and $\Delta i_0$ with respect to time are shown in Figs. 11 and 12 when the two PWM control strategies are employed respectively. It can be seen from Figs. 11 and 12 that the dynamic response time of the 3DSCH control is faster than the 3DSVM method. On the whole, the total performance of the 3DSVM is better than the 3DSCH control when its switching frequency is smaller than half of that of 3DSCH control. Furthermore, the switching loss of the 3DSVM method is lower than that of the 3DSCH method.

## V. EXPERIMENTAL RESULTS

A three-phase four-wire shunt power quality compensator prototype is implemented, in which a three-level NPC inverter

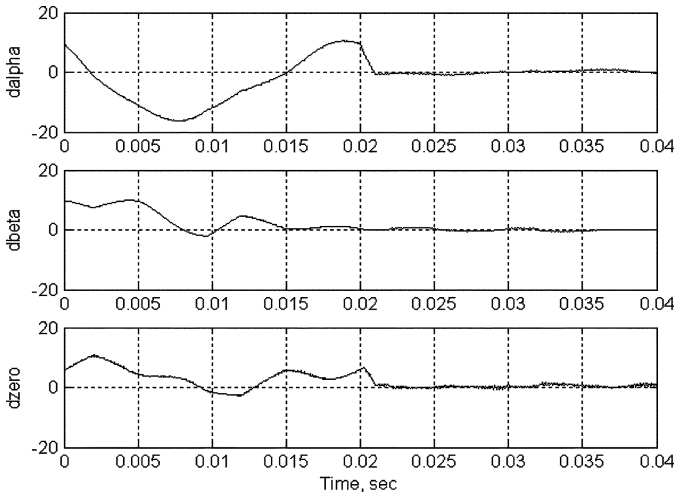


Fig. 12. Compensation error by using 3DSVM.

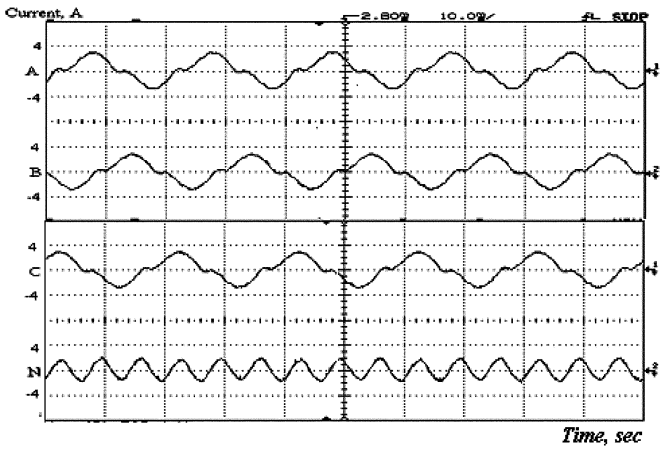


Fig. 13. Three-phase balanced source current before compensation.

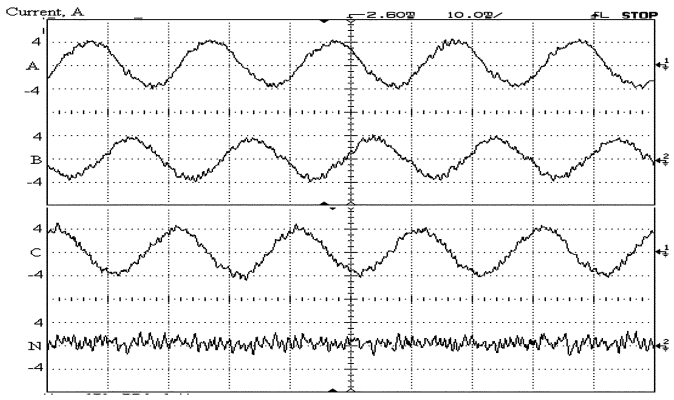


Fig. 14. Three-phase balanced source current after compensation by 3DSCH.

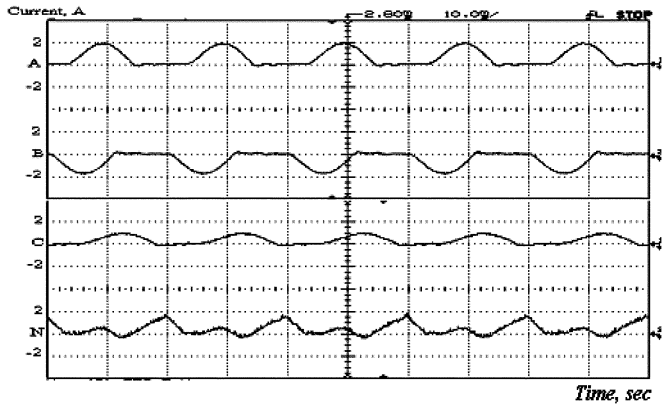


Fig. 15. Three-phase unbalanced source current before compensation.

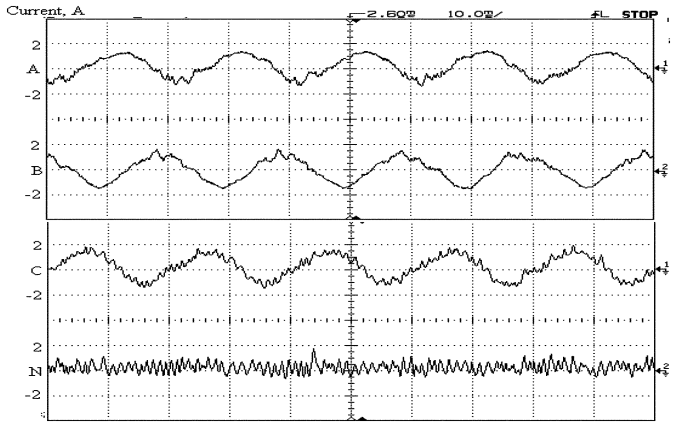


Fig. 16. Three-phase unbalanced source current after compensation by 3DSCH.

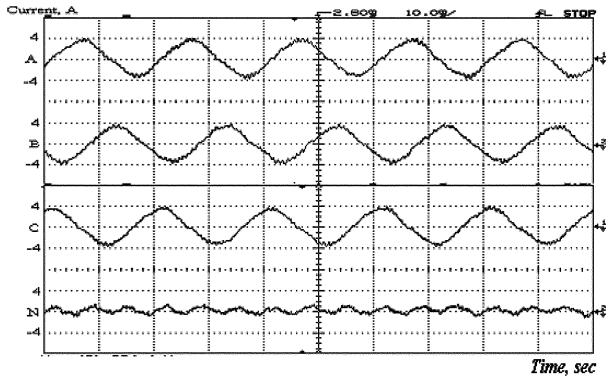


Fig. 17. Three-phase balanced source current after compensation by 3DSVM.

is used. The RMS value of source voltage is 55 V and $Lc =$ 6 mH, $V_{\rm dc} = 130$ V, $C = 10$ mF.

First, the 3DSCH method is applied to control the shunt power quality compensator. The three-phase balanced nonlinear load currents before and after compensation are shown in Figs. 13 and 14, respectively. The three-phase unbalanced load currents before and after compensation are shown in Figs. 15 and 16, respectively.

The proposed generalized 3DSVM control strategy is implemented with 5-KHz sampling frequency by a TMS320F2407 DSP controller. The current after compensation is shown in Figs. 17 and 18, respectively, from which it can be seen that current harmonics and neutral current are all compensated. The reactive power compensation is illustrated in Fig. 19, in which the power factor at the source side is near unity after compensation. The dynamic performance of the compensator is illustrated in Fig. 20, so that the validity of the proposed 3DSVM is proven.

The compensation performance of the 3DSCH and 3DSVM are compared in experiments too. The phase current THD values and the RMS values of neutral current are all listed in Table V. Results indicate that the 3DSVM control can obtain better performance than 3DSCH control when its switching frequency is

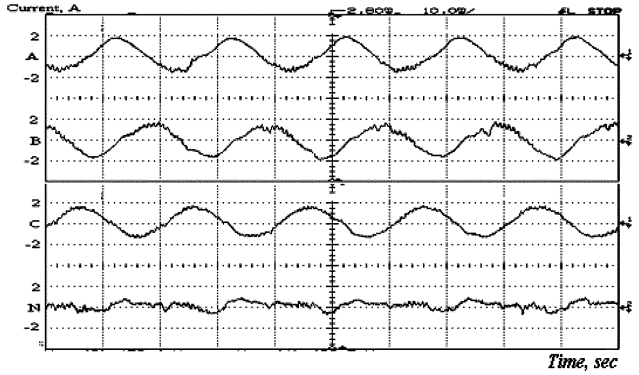


Fig. 18. Three-phase unbalanced source current after compensation by 3DSVM.

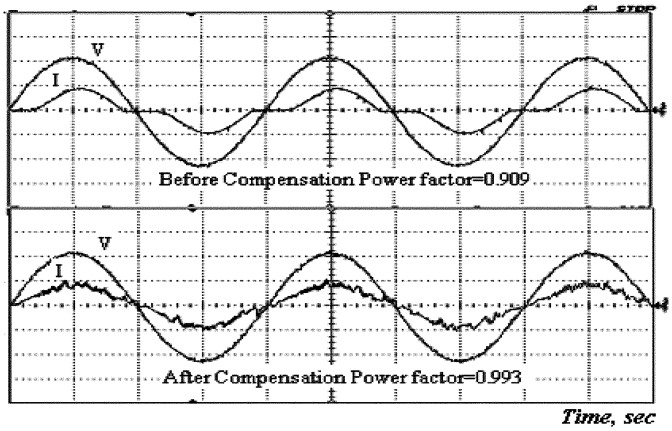


Fig. 19. Power factor compensation by 3DSVM.

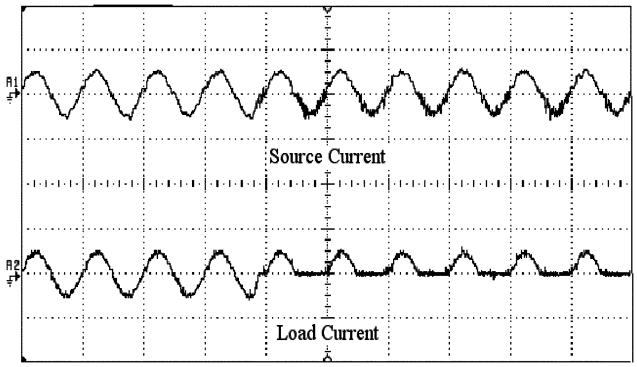


Fig. 20. Dynamic performance by using 3DSVM.

TABLE V
COMPARISON OF THREE-LEVEL 3DSVM AND 3DSCH

| | Parameters | THD% | | | RMS(A) |
|---|---|---|---|---|---|
| | Systems | A | B | C | N |
| Three phase Balanced load | Before Compensation | 26.34% | 24.11% | 24.87% | 1.205 |
| | By 3DSVM Technique | 7.698% | 6.599% | 7.560% | 0.441 |
| | By 3DSCH Technique | 6.940% | 7.025% | 6.313% | 0.753 |
| Three phase Unbalanced load | Before Compensation | 43.40% | 42.83% | 33.90% | 1.205 |
| | By 3DSVM Technique | 11.75% | 12.20% | 5.414% | 0.640 |
| | By 3DSCH Technique | 13.97% | 10.01% | 14.95% | 0.936 |

lower, and the corresponding switching loss of the 3DSVM is also lower.

## VI. CONCLUSION

This paper focuses on the application of three-level NPC inverters in a shunt power quality compensator for a three-phase four-wire system. First, a comparative study between the three-level four-leg NPC inverter and the three-level NPC inverter is presented. Results indicate that both the two inverter structures can be used to compensate neutral currents in a three-phase four-wire system. The four-leg inverter has higher neutral current compensation capability. However, its initial cost is high and the PWM control strategy for the four-leg inverter is complicated. Hence, the three-level NPC inverter is used to implement a shunt power quality compensator in this paper.

The SVM techniques for a multilevel inverter lead to large tables of vectors, e.g., there are, in total, 27 voltage vectors for a three-level NPC inverter. A generalized 3DSVM is proposed in this paper, in which the reference voltage vector is decomposed to an offset vector and a two-level vector. No matter how many vectors exist in a multilevel space vector allocation, the important issues of 3DSVM, such as identification of neighboring vectors and dwell times calculation, are all settled by a general two-level 3DSVM control. The zero-sequence component of each vector is considered, so that the neutral current compensation can be implemented. Furthermore, the control algorithm of the proposed 3DSVM is independent of the levels of the inverter and its computational cost is always the same.

Both simulation results and experimental results are given to show the validity of the proposed control strategy. The neutral current can be compensated simultaneously with current harmonics, unbalance current and reactive current. Comparisons with 3-D Sign cubic hysteresis control strategy [10] are also achieved in the paper. Results indicate that the proposed 3DSVM can obtain better performance than the 3DSCH control when its switching frequency is much lower than that of 3DSCH control.

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